Reg.No.:								

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 5026

M.E. / M.Tech. DEGREE END-SEMESTER EXAMINATIONS – DECEMBER 2019
First Semester
Computer Science and Engineering
P15CS102 - ADVANCED COMPUTER ARCHITECTURE
(Regulation 2015)

Time : Three Hours Maximum : 100 Marks

Answer ALL the questions

PART – A

(10 x 2 = 20 Marks)

1. What is an Accumulator Architecture?
2. What are data dependences and hazards?
3. Describe Flynn's classification of parallel computers.
4. What are limitations of instruction level parallelism?
5. Differentiate between WAR and RAW hazards.
6. Explain the idea behind dynamic scheduling.
7. What all are the hardware support for exposing parallelism?
8. What is multiprocessor cache coherence?
9. What are the types of storage device?
10. What is meant by false sharing?

PART – B

(5 x 13 = 65 Marks)

11. a) What are major hazards in a pipeline? Explain data hazard and methods to minimize data hazard with examples.

(OR)

b) Discuss the various addressing modes with an example for each.

12. a) How to overcome the data hazards with dynamic scheduling? What are the major hurdles of pipelining?

(OR)

b) How to enhance the loop level parallelism? What is the basic compiler technique for exposing ILP?

13. a) How did single core architectures exploit data level parallelism? Explain models of memory consistency in details.

(OR)

b) How do exploit ILP using multiple issues and dynamic scheduling? What are limitations of ILP-Hardware over Software Speculation

14. a) Explain the different taxonomy of parallel architecture. Describe distributed shared memory architecture in details.

(OR)

b) What is the concept of simultaneous multi threading? Explain performance of symmetric shared memory multiprocessors.

15. a) List the methods for providing synchronization in threads. Explain basic schemes for enforcing coherence.

(OR)

b) Explain the performance of symmetric shared memory multiprocessors. Explain the types of basic cache optimization.

PART – C

(1 x 15 = 15 Marks)

16. a) Discuss the concept of virtual memory and explain how a virtual memory system is implemented, pointing out the hardware and software support.

(OR)

b) Explain the directory based cache coherence for a distributed memory multi processor system along with state transition diagram. List two approaches to cache coherence protocol.